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Probing Molecular Packing at Engineered Interfaces in Organic Field Effect Transistor and Its Correlation with Charge Carrier Mobility

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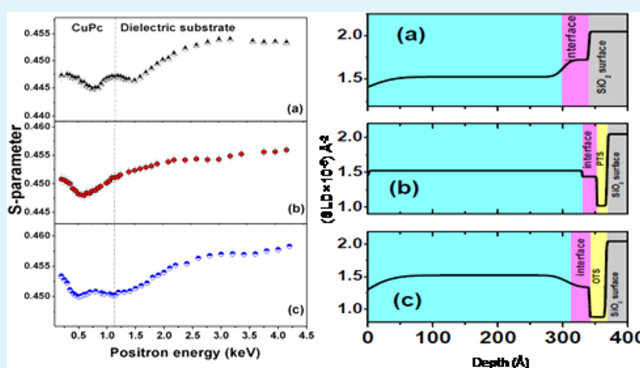
ABSTRACT: Surface engineering of SiO_2 dielectric using different self-assembled monolayer (SAM) has been carried out, and its effect on the molecular packing and growth behavior of copper phthalocyanine (CuPc) has been studied. A correlation between the growth behavior and performance of organic field effect transistors is examined. Depth profiling using positron annihilation and X-ray reflectivity techniques has been employed to characterize the interface between CuPc and the modified and/or unmodified dielectric. We observe the presence of structural defects or disorder due to disorientation of CuPc molecules on the unmodified dielectric and ordered arrangement on the modified dielectrics, consistent with the high charge carrier mobility in organic field effect transistors in the latter. The study also highlights the sensitivity of these techniques to the packing of CuPc molecules on SiO_2 modified using different SAMs. Our study also signifies the sensitivity and utility of these two techniques in the characterization of buried interfaces in organic devices.



KEYWORDS: *positron annihilation spectroscopy, organic semiconductors, self-assembled monolayer, interface molecular packing, field effect mobility*

INTRODUCTION

Organic field effect transistors (OFETs) are shown to be useful in a variety of applications such as smart card, flat panel displays, sensors, electronic identification barcodes, etc. One of the key aspects in the existing OFETs is the relatively low charge carrier mobility, which for thin film devices is partially caused by the large grain boundary resistance.[1,2] Recently, Yuan et al. have reported a highest mobility of ~43 $cm^2\ V^{-1}\ s^{-1}$ using the compound 2,7-dioctyl[1]benzothieno[3,2-*b*][1]-benzothiophene (C8-BTBT).[3] Extensive studies have been conducted to improve charge carrier mobility in OFETs, which is still >1 order of magnitude lower than that of the silicon-based transistors. Since charge carriers in OFETs are transported between the conjugated molecules very close to the organic semiconductor (OSC)−gate dielectric interface, i.e., within approximately a few monolayers of OSC film, the performance of the devices depends on grain size, structural defects, relative orientation, and ordering of molecules within these few monolayers. In most of the OFETs, inorganic oxides like SiO_2 or Al_2O_3 are employed as gate dielectrics because of their well-studied dielectric properties. These oxide dielectrics offer a large number of interface traps on the surface that additionally cause a major hindrance to charge transport.[4,5] There are many reports in the literature discussing the role of hydroxyl groups on the metal oxide surfaces acting as electron trap centers and, hence, influencing the functioning of OFET devices.[5−7] Passivation of these hydroxyl groups with polymers or self-assembled monolayers (SAMs) with nonpolar groups is an efficient and commonly employed technique for eliminating the effect of electron trap centers.[7−9] Such a passivation procedure also aids in screening the dipoles of the polar surfaces and helps in improving the morphology of the film.[9,10] Use of SAM is more advantageous than that of polymers because of the high density of interchain cross-linking that helps to reduce the surface roughness, thereby improving the molecular ordering at the interface. The thickness of SAMs are generally within a few nanometers (<3 nm) and do not decrease the capacitance of the dielectric. While spin coating polymers on the SiO_2 surface leads to an increase in the thickness of the dielectric, thereby reducing the capacitance, which in turn can affect the charge mobility and operating voltage of OFETs. Additionally, the surface energy of the dielectric can also be easily modified using SAMs with different functional groups, influencing the nucleation and growth mechanism of the OSC.[11,12]

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It is well reported in the literature that the molecular alignment, growth mode, grain size, and crystalline structure of OSC thin films depend on molecule−substrate and molecule−molecule interactions, which are primarily determined by the surface energy of the dielectric.[13,14] Some studies on pentacene and copper phthalocyanine (CuPc)-based OFETs have reported that larger grains and higher mobility could be obtained by matching the surface energy of the dielectric and OSC.[15,16] In contrast, some groups have reported improved carrier mobility with reduced grain size.[17,18] Liscio et al. have studied the effect of defects in molecular organization on the charge transport in OFETs that arise from the specific growth conditions of OSC.[19] All these studies clearly imply the crucial role of interface properties understanding which is highly essential for further development of high-performance devices. Even though the influence of morphology, molecular ordering, and grain size on charge transport have been well explored, the influence of the dielectric on the origin of disorder during the initial stages of growth and its effect on charge transport needs to be investigated further. This provides strong motivation for probing interfacial properties necessitating search for suitable tools and techniques.

Growth modes of OSCs are mostly examined using scanning probe microscopy techniques like atomic force mircoscopy (AFM).[12,14,17] Photoemission electron microscopy (PEEM), in which individual layers are monitored during the growth of the film,[20] has also been employed in the past for such studies. Massari et al. have recently demonstrated the use of a sum frequency generation technique as a powerful tool for understanding molecular growth at these technically important interfaces in organic devices.[21] In OFET devices, especially top contact devices, even though charge accumulation and transport occur in the initial few monolayers, OSC films are generally maintained thicker than a few monolayers to prevent diffusion of metal electrodes into the film up to the interface. For such devices with thicknesses of more than a few monolayers, device performance is mostly correlated with the morphology seen from the top of the bulk layer using AFM, leading to erroneous conclusions, because interface properties can be different from the bulk properties. To study the growth mechanisms at the interface, OSC films have to be deposited sequentially and the morphology has to be examined using AFM at each step, but this method can also pose some errors since thickness-dependent structural evolution and change in interface conditions, i.e., modification of initial monolayers of OSC films with the subsequent deposition of top layers, are expected.[22−24] Therefore, it is essential to probe buried interfaces in these devices using suitable nondestructive techniques to ascertain the correlation between interface conditions and device performance. X-ray reflectivity is one such tool where reflectivity measurements in specular mode map the variations in electron density along the direction normal to the surface. This can provide information about the thickness of the layers and surface/interface properties with high sensitivity, making it well suited to study the characteristics of ultrathin organic multilayers and buried interfaces with nanometer accuracy.[25,26]

DC beam-based positron annihilation spectroscopy (PAS) has been uniquely used by our group to probe interfaces in organic multilayers.[27] The sensitivity of the technique lies in the ability of the positron to get localized in low-electron density regions (defects/open volumes) owing to the repulsive force between the positron and ion cores that helps in probing atomic order defects in materials with sensitivity in the range of a few parts per million. The underlying manifestations in positron annihilation spectroscopy are the increase in the lifetime of the positron and narrowing of the momentum distribution of the annihilation photon (measured from the Doppler broadening of annihilation γ radiation) when the positron is trapped in the defect. Beam-based PAS, employing monoenergetic positrons, enables probing surfaces, molecular ordering/packing at buried interfaces, and structural variations along the direction normal to the surface in thin films.[26,28]

In this study, a positron annihilation technique has been used to probe the buried interface between the OSC (CuPc) and gate dielectric (SiO_2) in OFETs. The effect of the surface energy of the dielectric, modified by engineering the OSC−dielectric interface using SAMs with different functional groups, on the growth behavior of OSC films has been examined. Our study highlights the potential of depth profiling using positron annihilation technique to probe molecular ordering and packing at the buried interfaces in OFETs. XRR has been used as a complementary technique to study the OSC−dielectric interface properties. There are only a few studies of the use of XRR as a tool to examine the growth behavior of OSC films in OFETs,[25,29,30]where some of them use this technique *in situ* during the film growth itself. Only negligible reports among those mentioned here employ XRR to study the difference in molecular ordering after SAM modification of the interface.[29,30] Even these studies do not discuss the effect of the surface energy of the dielectric on growth behavior. We have shown that the positron annihilation technique, complemented with XRR, can be successfully employed to study the influence of the surface energy of the dielectric on the growth behavior of OSC films within the few monolayers near the dielectric surface in OFETs. We have also shown excellent correlation of device performance with the molecular packing at the OSC−dielectric interface, verified using these techniques.

■ EXPERIMENTAL SECTION

A highly doped *n*-type (100) silicon wafer (0.01−0.015 Ω cm) was used as a substrate and gate electrode, with the 230 nm thermally grown SiO_2 layer acting as the gate dielectric. The surface of SiO_2/Si substrate was modified with SAMs of phenylhexyltrichlorosilane (PTS) and octadecyltrichlorosilane (OTS). For this purpose, Piranha-cleaned substrates were immersed in a freshly prepared 0.25 mM PTS solution in toluene for 3 h and a 0.5 mM OTS solution in toluene for 24 h, in an argon-filled glovebox (relative humidity and oxygen levels of <1 ppm).[12,31] CuPc purchased from Sigma-Aldrich was thermally evaporated on unmodified SiO_2/Si (film 1), SAM modified viz. PTS/SiO_2/Si (film 2), and OTS/SiO_2/Si (film 3) substrates maintained at room temperature. The evaporation rate and thickness of the film were maintained at 0.5−1 Å/s and 30 nm, respectively, which were measured by a quartz crystal monitor. To study the interface conditions, 2 nm thick CuPc film was also evaporated on all the three substrates in a similar fashion. The quality of monolayers was verified by measuring the thickness using an optical ellipsometer (SENTECH Germany) and water drop contact angle (Data Physics Instrument). The morphology of CuPc films (30 and 2 nm) and dielectric (SiO_2/Si) surface roughness were verified by atomic force microscopy (NT MDT SOLVER, model P47H). The cantilever tip used for the measurements was a super sharp DLC tip (model NSG10_DLC) with a radius of curvature of 1−3 nm. The force constant was 8.7 N/m, and the fundamental resonance frequency was 193.6 kHz. The measurements were taken in semicontact or intermittent mode, which gives artifact free images. The structure and crystalline nature of CuPc films were determined by X-ray diffraction measurements using a RIGAKU analytical X-ray diffraction system (model RINT 2000 Dmax) carried out using Cu Kα radiation. Top

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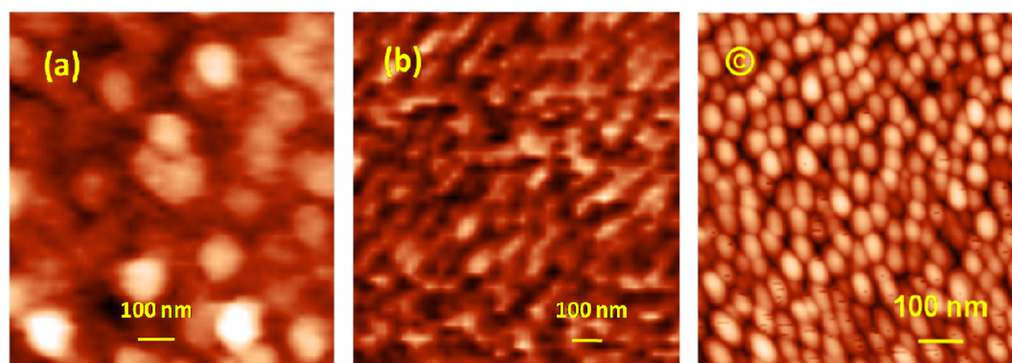

Figure 1. AFM images of CuPc films (30 nm) on (a) SiO_2/Si, (b) PTS/SiO_2/Si, and (c) OTS/SiO_2/Si dielectrics indicating different grain sizes.

contact OFET devices were prepared by thermally evaporating gold through a shadow mask for source (S) and drain (D) electrodes above the CuPc film with channel length and channel width of 25 μm and 2 mm, respectively. For capacitance measurements, gold electrodes with an area of 25×10^{-4} cm^2 were deposited on gate dielectrics through a shadow mask to form a Au/dielectric/Si(n^{2+}) structure. Capacitance and current−voltage ($I-V$) characteristics were measured in air at room temperature using an Agilent 4284A LCR meter and Keithley voltage source/current meter (model 6487), respectively.

Beam-based Doppler broadening of annihilation γ-radiation (511 keV) was carried out in the positron incidence energy range from 0.2 to 18.2 keV. Doppler broadening of 511 keV is measured by a HPGe detector with resolution of 2.0 at a 1332 keV photopeak of ^{60}Co. The detector is positioned at 90° to the incident beam, and half a million counts were acquired under the 511 keV photopeak at each energy. Doppler broadening (ΔE) of annihilation radiation ($\Delta E = cp_L/2$, where p_L is the longitudinal momentum component of the annihilating electron−positron pair) is characterized by line shape parameter S, defined as the ratio of integral counts within ~2.0 keV energy window centered at 511 keV to the total photo peak area. The narrow window of ~2 keV primarily represents valence electrons. In the event of positron trapping in an open volume defect, the overlap of the positron is reduced with low-momentum valence electrons as well as high-momentum core electrons, the reduction being much greater in the latter case. This leads to an effective narrowing of the momentum distribution manifested as an increase in the S parameter. In addition to the S parameter, the positron lifetime, which depends on the electron density at the trapping/annihilation site, can also be used to identify trapped positron states. The reduced electron density at the trapping site (open volume defect/vacancy) results in an increase in positron lifetime. The S parameter and positron lifetime depend on the density of valence electrons (n_{val}) available in the volume defined by size parameter r_s given as[32] $(4\pi/3)r_s^3 = n_{val}^{-1}$ and can be qualitatively related to the molecular packing density in organic systems. Positron lifetime measurements were taken at two different incident energies, viz. 0.8 and 1.1 keV, using the pulsed positron beam facility at the National Institute of Advanced Industrial Science and Technology (Tsukuba, Japan).[33] The implantation depth of the positron is related to the incident energy by the relation $z_0 = AE^n/\rho_d$, where z_0 is expressed in nanometers, E is the positron energy in kiloelectronvolts, ρ_d is the density of the medium in grams per cubic centimeter, $n \approx 1.6$ for positron incident on most of the materials, and A is a material-dependent constant. On the basis of this and using an approximate density of 1.6 g/cm^3, positron energies of 0.8 and 1.1 keV correspond to positron implantation in the subsurface (~18 nm) and near-interface region (~30 nm), respectively.

XRR measurements were carried using a laboratory X-ray source using Cu Kα radiation (λ = 0.154 nm). In this technique, the intensity of X-rays reflected specularly (i.e., angle of incidence = angle of reflection) from the sample surface is measured as a function of wave vector transfer q (Å^{-1}), perpendicular to the reflecting surface. Here q is equal to $(4\pi/\lambda)\sin\theta$, where λ is the wavelength of incident beam and θ is the grazing angle of incidence with respect to the sample surface. Reflected intensities were collected with the rotating anode X-ray source in $\theta-2\theta$ scanning geometry. The experimental reflectivity data were fitted with a theoretical model consisting of various slabs or layers with depth-dependent electron scattering length density (SLD) ρ (in units of Å^{-2}) averaged over lateral dimensions of the sample, from which the density gradient in the layered structure was extracted. Scattering length densities are related to the atomic number densities in a multicomponent system through the following equation:

$$\rho = r_e \sum_i N_i f_i \tag{1}$$

where r_e (= 2.818 fm) is the classical electron radius and N_i and f_i are the depth-dependent number density per unit volume and the real anomalous dispersion factor, respectively, of the ith element.

RESULTS AND DISCUSSION

Structural Characterization of SAM and CuPc Films. Thicknesses of SAM monolayers measured using ellipsometry were found to be 1.4 ± 0.1 and 2.6 ± 0.2 nm for PTS and OTS, respectively,[12,31] which are close to their theoretically calculated values of 1.45 and 2.62 nm, respectively. The water drop contact angle measured on the freshly cleaned SiO_2/Si was less than 10°, which increased to 87 ± 1° and 108 ± 1° after the deposition of PTS and OTS, respectively, indicating the conversion of the hydrophilic SiO_2 surface to a hydrophobic surface. The average surface roughness of the SiO_2 dielectric before and after PTS and OTS treatment, as verified by AFM, was found to be ~1.2, ~0.3, and ~0.1 nm, respectively. This indicates significant reduction of surface roughness after the modification of the dielectric surface with SAMs. The surface morphologies of 30 nm thick CuPc films 1−3 examined by AFM are shown in Figure 1. The grain size of film 1 is >150 nm, while that of film 3 is reduced to <50 nm. On the other hand, film 2 shows well-connected grains of size intermediate between those of the grains of films 1 and 3.

Figure 2 shows the XRD patterns for films 1−3 showing a single major peak corresponding to the (200) plane of the α-phase of CuPc. This peak indicates an edge-on orientation of CuPc molecules with their stacking axis parallel to the substrate surface. This type of stacking is known to yield better charge transport along this direction.[12,31] The peak was found to be sharp, having full widths at half-maximum (fwhms) of 0.23° and 0.21° for films 2 and 3, respectively, while a broader peak with a fwhm of 0.28° was observed for film 1, indicating improved crystallinity of CuPc films on SAM-modified dielectrics.

Interface Characterization. *AFM.* The morphology of the ~2 nm thick CuPc film (slightly more than one monolayer thick CuPc, as the height of the upright standing CuPc molecule in the edge-on configuration is ~1.3 nm)[34] grown on

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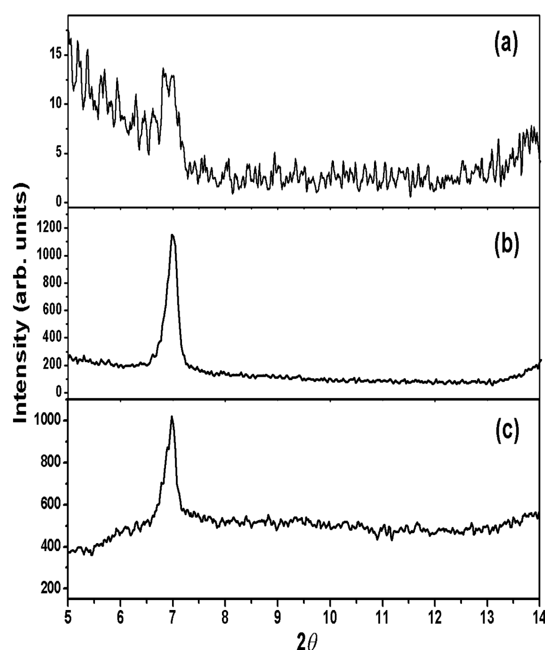

Figure 2. XRD patterns of CuPc films grown on (a) SiO_2/Si, (b) PTS/SiO_2/Si, and (c) OTS/SiO_2/Si dielectrics indicating the crystalline nature of the films.

unmodified and SAM-modified dielectrics was verified using AFM to examine the growth modes of the CuPc film near the dielectric surface. Figure 3 shows the AFM images and the corresponding height profiles of the 2 nm CuPc film on the unmodified and SAM-modified dielectrics (films 1−3). The height profiles indicate that the film grown on the unmodified and PTS-modified dielectric follow layer plus island growth mode (Frank-van der Merwe mechanism) with grain size being smaller on the unmodified dielectric (film 1) similar to the growth modes reported previously.[12,34,35]

It can be seen that the height of the largest peak in the roughness profile for the CuPc film on unmodified SiO_2 is ∼2.5 nm (Figure 3a). This suggests that after completion of first monolayer, CuPc molecules grow in a vertical direction. The roughness profile in Figure 3a also shows that there are many peaks with a height of <1.3 nm, implying that these peaks should correspond to the first monolayer. The height of some of these peaks is as small as 0.5 nm, which is much less than that of an upright standing molecule in fully edge-on configuration. Since only strongly tilted molecules can give rise to such small peak heights, it can be suggested that CuPc molecules on the SiO_2 surface could be oriented with a more tilted configuration resulting in an array of randomly oriented molecules near the dielectric surface. In the case of the PTS-modified dielectric, the highest peak is ∼3 nm, indicating island formation. At other locations where such islands are not formed, the roughness profile shows a peak height of ∼1.1 nm, close to one monolayer height indicating that molecules are more upright in the initial monolayer, with a grain size much larger than that on unmodified SiO_2. In the case of the OTS-modified dielectric, CuPc molecules grow in island mode (Volmer−Weber) with the height of islands extending up to ∼15 nm (much higher than 2 nm), with no marked peaks with smaller heights, close to or less than one monolayer.

Positron Annihilation Studies. Figure 4 shows the S parameter profile for films 1−3 normalized with respect to the average S value in the silicon substrate. The implantation depth of 1.1 keV positrons in the CuPc film is ∼30 nm, which corresponds to the depth of the CuPc−dielectric interface. The SiO_2 layer (∼230 nm) corresponds to the depth primarily to the positron implantation energy between 1.1 and 6 keV. The slight variation in the S parameter in the SiO_2 region across the three films is probably due to the minor variation in the physical properties of the oxide layer.[36,37] The more critical parameter is the SiO_2 surface roughness that is seen to be similar in all cases (∼1.2 nm).

Figure 5 shows the S parameter profiles for positron energies up to 4.5 keV for better illustration of the differences in the CuPc region in the three cases. The S parameter profiles for films 2 and 3 are seen to be higher than that of film 1; e.g., at E

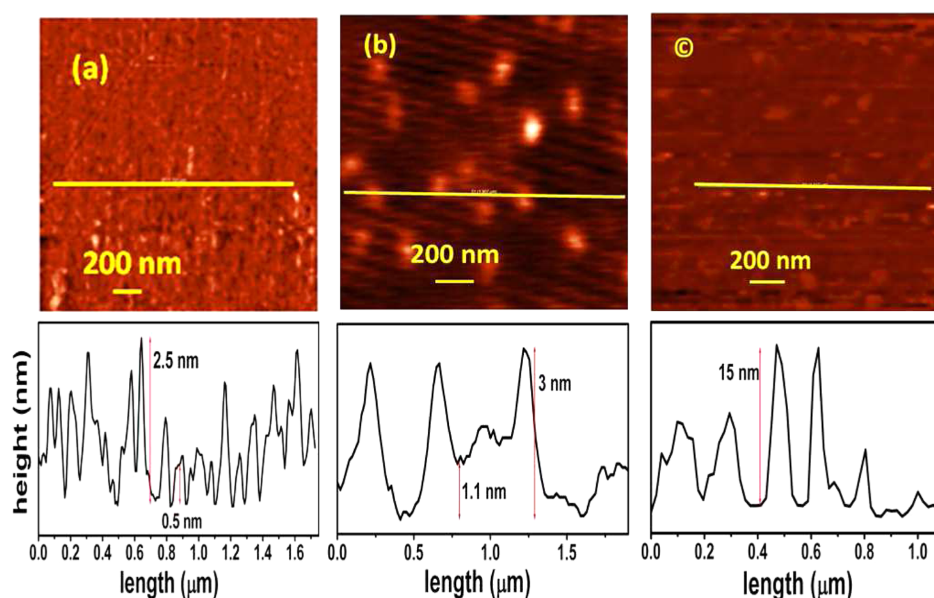

Figure 3. AFM images of ∼2 nm CuPc films grown on (a) SiO_2/Si, (b) PTS/SiO_2/Si, and (c) OTS/SiO_2/Si dielectrics with their corresponding height profiles indicating the growth behavior of CuPc molecules on the dielectric surfaces.

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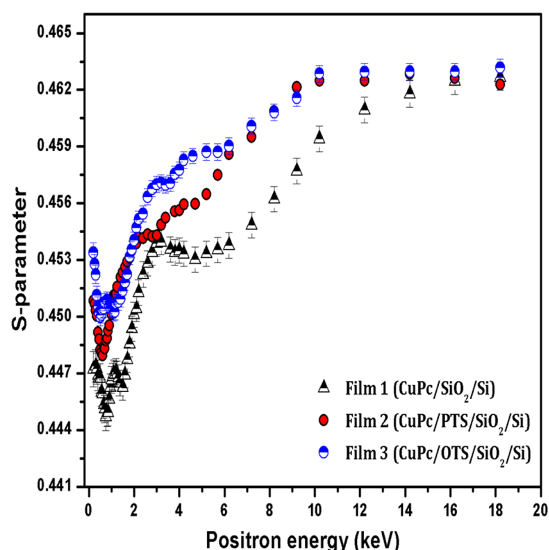

Figure 4. *S* parameter profile for CuPc films on unmodified and SAM-modified dielectrics.

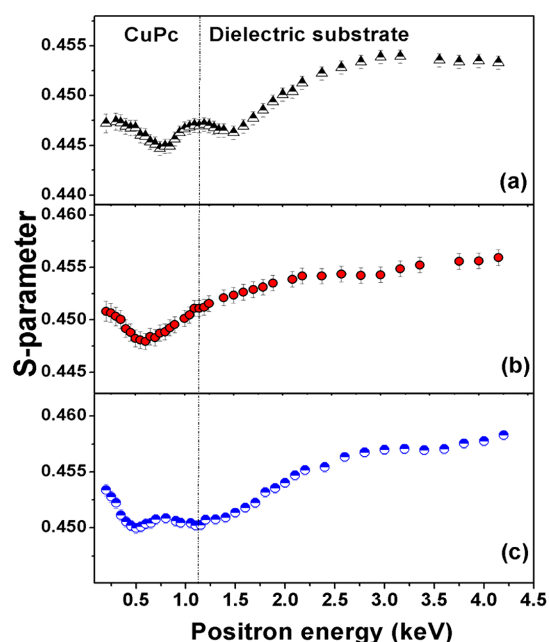

Figure 5. *S* parameter profile (up to 4.5 keV) for CuPc films on (a) SiO_2/Si, (b) PTS/SiO_2/Si, and (c) OTS/SiO_2/Si dielectrics. The dotted line (at 1.1 keV) shows the interface between the CuPc and dielectric.

= 0.8 keV corresponding to approximately the middle region of the CuPc film, the *S* parameter for films 1−3 are 0.445, 0.449, and 0.451, respectively, which can be ascribed to the difference in the morphologies of the films as seen from AFM (Figure 1). Since the films have different morphologies, the difference in the *S* parameter cannot be directly correlated to defect density. However, the individual profile can provide information about the structural inhomogeneities/defect density profile of the film. The *S* parameter shows a decreasing trend in the subsurface region (∼0.2−0.7 keV) for all the films, indicating the crystalline nature of the films, as observed in our earlier study on OSC multilayers.[27] However, the profiles are different in the near-interface region (∼0.7−1.1 keV). In the case of film 1, the near-interface region shows an increase in the *S* parameter with a prominent humplike feature around 1.1 keV. The high value of the *S* parameter at 1.1 keV indicates the trapping of the positron in defects indicating a distinct interface layer near the dielectric surface. It has been reported that surface energies of CuPc, SiO_2, OTS/SiO_2, and PTS/SiO_2 are ∼35.1, ∼68.5, ∼32.9, and ∼38.5 mJ/m^2, respectively.[12,38] The higher surface energy of the unmodified dielectric (SiO_2/Si) compared to that of CuPc and high surface roughness lead to a disordered arrangement of molecules at the surface, giving rise to structural defects within few monolayers near the dielectric surface. AFM study also indicates disorientation of the molecules at the surface of the unmodified dielectric. Unlike film 1, the near-interface regions in films 2 and 3 (modified dielectrics) do not show a humplike feature around 1.1 keV (Figure 5), as seen from the smooth variation the *S* parameter at that energy, indicating the absence of a distinct interfacial region. However, the *S* parameter profiles in the near-interface region for the two cases are markedly different. In the case of film 2, the *S* parameter shows an increasing trend with values approaching that of the SiO_2 layer, while film 3 shows an almost flat *S* parameter trend. Since the PTS and OTS layer thickness is 1.4 and 2.6 nm, respectively, their contribution to the *S* parameter is very small to account for the observed difference. Therefore, the difference in the *S* parameter profiles (in the near-interface region) in films 2 and 3 can be attributed to the molecular ordering and/or packing in this region because of the difference in the surface energy of the SAM-modified dielectrics as also observed in the AFM study.

The molecular packing is also expected to influence positron lifetime in organic materials. The average positron lifetimes at two positron implantation energies, viz. 0.8 and 1.1 keV, corresponding to the subsurface and near-interface region, respectively, are listed in Table 1. The positron lifetime and *S* parameter follow the same trend from the subsurface to near-interface region in all the films as expected, because of the dependence of both these parameters on the density of valence electrons available at the trapping site.[32] This implies higher positron lifetime would lead to a higher *S* parameter and vice versa. The positron lifetime variation can be used to get information about the molecular packing/structural inhomogeneities as a function of the thickness of the films. In the case of films 1 and 2, there is an increase in the *S* parameter from the subsurface to near-interface region, consistent with the increase in average positron lifetimes in the two regions, while in the case of film 3, there is no significant change in lifetime at the two energies, consistent with a similar value of the *S* parameter (Figure 5). This indicates that the molecular packing/stacking arrangement changes from the subsurface to near-interface region in the case of films 1 and 2, whereas there is no significant variation in the case of film 3. It indicates that the molecular stacking arrangement propagates until ∼10−15 nm

Table 1. Average Positron Lifetimes at Subsurface and Near-Interface Regions

film specification	subsurface region (E = 0.8 keV) (ns)	near-interface region (E = 1.1 keV) (ns)
CuPc/SiO_2/Si (film 1)	0.333 ± 0.002	0.340 ± 0.002
CuPc/PTS/SiO_2/Si (film 2)	0.343 ± 0.002	0.354 ± 0.002
CuPc/OTS/SiO_2/Si (film 3)	0.343 ± 0.002	0.341 ± 0.002

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from dielectric surface (the 0.8 keV energy approximates to ∼18 nm depth from the surface) in the case of film 3. This is consistent with the AFM study (Figure 3) that indicates the growth of three-dimensional (3D) islands up to ∼15 nm from the surface. The average positron lifetime is lower in the subsurface than in the near-interface region in film 2, indicating the enhancement of molecular packing with the increase in the thickness of the film because of the reduced effect of molecule−substrate interaction. As the thickness of the film increases, the effect of molecule−substrate interaction becomes weaker and the interaction between the molecules dominates, leading to an increase in molecular packing density within the grains.[39] In the case of film 1, the positron lifetime is reduced marginally in the subsurface region compared to the near-interface region approaching the positron lifetime in bulk phthalocyanine.[40] The study shows that *S* parameter and lifetime measurements together can provide a better understanding of molecular packing and, hence, growth behavior at the interfaces.

X-ray Reflectivity. The left panel of Figure 6 shows experimental XRR profile data (○) and the fits (—) for

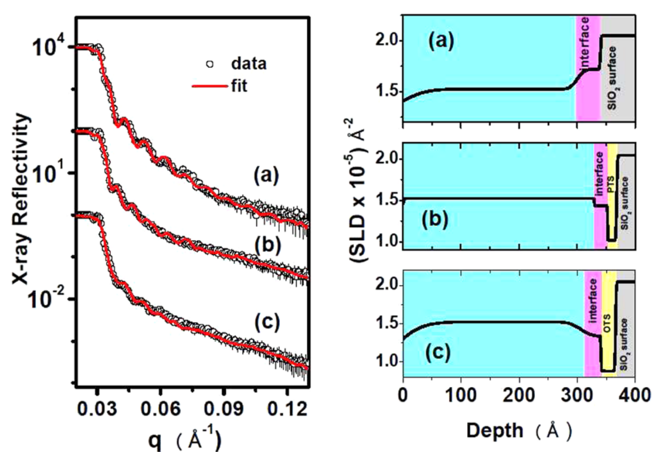

Figure 6. XRR (left) and SLD (right) profiles for (a) SiO_2/Si, (b) PTS/SiO_2/Si, and (c) OTS/SiO_2/Si dielectrics. The SLD profiles indicate different layers, modeled to fit the observed XRR profiles.

CuPc films grown on unmodified and modified dielectrics (films 1−3). The plots have been vertically displaced for the sake of clarity. The physical structure of the films was modeled as CuPc/intermediate layer/unmodified (or, modified) SiO_2 (230 nm)/Si to get the best fit to the profiles. The right panel in the same figure shows the SLD profiles for all the films. Position zero of the depth axis in the right panels indicates the air−film interface. The SiO_2 layer with a thickness of 230 nm has been truncated to highlight the intermediate (or interface, used synonymously here) layer. The derived parameters for layer thickness and number density of atoms at the interface layer (intermediate layer) are listed in Table 2. The SLD profiles for the films clearly show the presence of the interface layer between CuPc and the unmodified/modified dielectric. However, the characteristics of the interface layer in terms of thickness, roughness, and number density of atoms are different, highlighting the variation in molecular ordering/packing at the surface of unmodified/modified dielectric. It is seen that in the case of film 1, the interface layer extends to ∼4 nm above the SiO_2 surface with a SLD slightly higher than that of CuPc, while in films 2 and 3, where the interface layer widths are 2.2 and 3.5 nm, respectively, the SLDs are slightly lower

Table 2. XRR Fitting Parameters for CuPc Films on SiO_2, PTS/SiO_2, and OTS/SiO_2 Dielectrics

film specification	CuPc layer thickness (nm)	CuPc interface layer (nm)	no. of atoms/cm^3 in the interface layer
CuPc/SiO_2/Si (film 1)	30	4	2.1×10^{21}
CuPc/PTS/SiO_2/Si (film 2)	33	2.2	1.75×10^{21}
CuPc/OTS/SiO_2/Si (film 3)	33	3.5	1.63×10^{21}

than that of CuPc. The number densities of atoms in the interface layer calculated using eq 1 are listed in Table 2. Owing to the strong molecule−substrate interaction and high surface roughness of unmodified dielectric (film 1), a random orientation of CuPc molecules exists during the initial stages of growth. Therefore, though the molecules have mostly edge-on configuration, many of them might be strongly tilted toward the substrate and possibly even with face-on orientation.[19] Such a random arrangement could lead to clustering of molecules within the few monolayers near the dielectric surface as schematically shown in Figure 7a. Since copper atoms (Cu) in these films act as the main scattering centers for X-rays, due to the random orientation and clustering of molecules in the interfacial region, X-rays see a clustering of several Cu atoms per unit volume leading to a higher SLD in this interface layer. The SLD profile for film 1 also exhibits a rising slope at both the air−CuPc and CuPc−interfacial layer interfaces, indicating the large degree of roughness associated with these surfaces. The presence of this distinct interface layer has also been observed in positron study, revealing it to be consisting of structural defects owing to the disorientation of the molecules.

On the other hand, in the case of film 2, the SLD profile falls sharply at CuPc−PTS interface, which is indicative of a very low degree of roughness. As discussed before, similar surface energies of CuPc and PTS lead to larger surface coverage of CuPc molecules on PTS with the stacking of molecules in a more ordered manner along the PTS surface (Figure 7b), resulting in a smooth interface. Such an ordered arrangement of molecules could be expected to prevent clustering of CuPc molecules. This could lead to a reduced number of scattering centers (Cu atoms) at the interface compared to that in bulk CuPc on this substrate and to that at the interface of film 1, resulting in a lower SLD.

In the case of film 3, the interface layer extends to ∼3.5 nm above the OTS monolayer with the SLD lower than that for films 1 and 2 and a much higher degree of roughness at the CuPc−OTS interface. Increased roughness generally indicates 3D island-type growth mode.[41] This agrees well with the expectation that on OTS/SiO_2, whose surface energy is much lower than that of CuPc, the 3D island-type growth mode (Figure 7c), with molecule−molecule interaction stronger than molecule−substrate interaction, with large voids between the grains is favored.[12] Stronger stacking of CuPc molecules in the edge-on configuration would clearly prevent disordered clustering of CuPc molecules in the initial monolayers (as expected in CuPc/SiO_2). Such a growth mode with large voids between the grains in the initial monolayers could cause the interface layer electron density in film 3 to be lower than that of CuPc on the unmodified (film 1) and PTS-modified dielectric (film 2).

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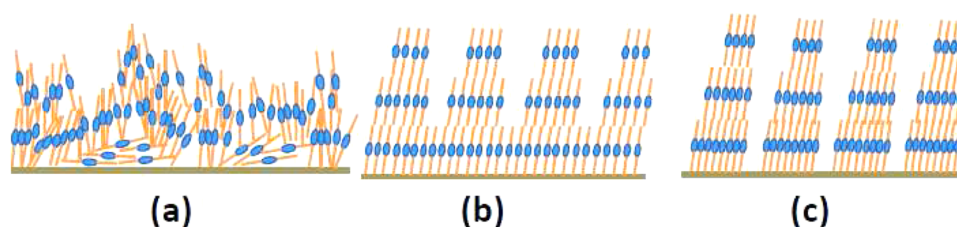

Figure 7. Schematic representation of growth of CuPc molecules at the surface of (a) SiO_2/Si, (b) PTS/SiO_2/Si, and (c) OTS/SiO_2/Si dielectrics indicating the effect of surface engineering on the growth behavior of CuPc on the dielectric surface.

Electrical Characterization of OFETs. The role of CuPc–dielectric interface structure as inferred from positron annihilation and XRR techniques on the OFET performance is verified by measuring the electrical characteristics of OFETs. Typical transfer characteristics of OFETs on unmodified and PTS- and OTS-modified dielectrics are shown in Figure 8. The gate voltage is scanned from +20 to −50 V fixing the drain voltage at −50 V corresponding to the saturation region. The field effect mobility of holes (μ_h) in the saturation region has been extracted from the plot of $I_D^{1/2}$ versus V_G using the equation

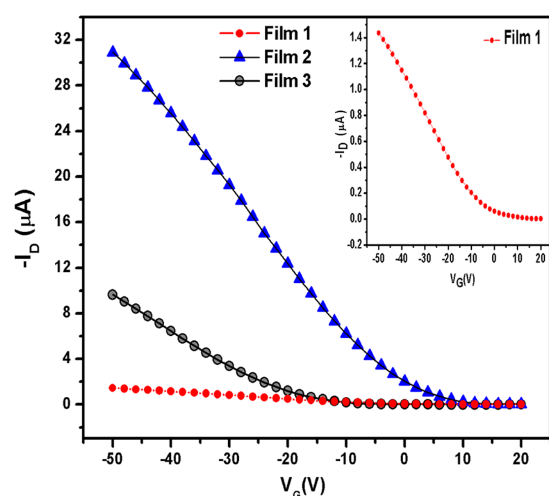

Figure 8. Transfer characteristics of OFETs on SiO_2/Si (film 1), PTS/SiO_2/Si (film 2), and OTS/SiO_2/Si (film 3) dielectrics. The inset shows the transfer characteristics of film 1 on an expanded scale.

$$I_D = \frac{WC_i}{2L}\mu_h(V_G - V_T)^2 \tag{2}$$

where L and W are length and width of the channel, respectively, C_i is the capacitance per unit area of the dielectric, I_D is the drain current, V_G is the gate voltage, and V_T is the threshold voltage.

The estimated μ_h values for OFET made on unmodified and PTS- and OTS-modified dielectrics are 0.0009 ± 0.00007, 0.02 ± 0.001, and 0.01 ± 0.002 $cm^2\ V^{-1}\ s^{-1}$, respectively. These results have been observed for at least 20 devices in each case. This shows that the performance of OFETs on modified dielectrics is better than that on unmodified dielectrics. The lowest mobility in the case of unmodified dielectric compared to modified (OTS/PTS) dielectrics is attributed to structural defects due to molecular disorder present at the interface between CuPc and the dielectric surface. These defects act as charge traps and thereby reduce the charge carrier mobility through the channel formed at the interface. The highest mobility observed for PTS devices could be attributed to well-ordered CuPc molecules in the initial layers with more two-dimensional (2D)-type growth with interconnected grains. Such a growth mode is generally known to enhance charge transport efficiency along the channel. In spite of stronger molecule–molecule interaction and hence better $\pi-\pi$ stacking facilitated by the lowest surface energy of OTS, charge carrier mobilities on OTS devices were lower than that on PTS. This could be due to the presence of voids between grains arising from 3D island-type growth of CuPc molecules in the case of the OTS-modified dielectric (film 3).

The OFET results are in agreement with earlier reports suggesting higher mobility for the more 2D growth mode of the OSC at the dielectric–semiconductor interface and for matching surface energies between the dielectric surface and OSC.[12,15] This shows that device performance correlates well with the growth properties at buried interfaces, studied using a positron technique and supported by XRR techniques.

CONCLUSIONS

The interface between the CuPc and dielectric (unmodified or SAM-modified) in OFET devices has been characterized using positron annihilation and XRR techniques. The sensitivity of the techniques to structural defects (PAS) and electron density contrast (XRR) at the interfaces aided in probing the molecular packing and growth behavior of OSC near the dielectric surface. The influence of the surface energy of the dielectric, varied by engineering the SiO_2 surface using different SAMs, on the molecular packing and growth behavior has been examined using these techniques and correlated with the performance of OFETs. The study has shown disordered growth of CuPc on the unmodified dielectric and ordered molecular packing on SAM-modified dielectrics, which is consistent with the observed high charge carrier mobility in OFETs in the latter. The studies could even further show the difference in packing of CuPc films on PTS and OTS substrates arising mainly due to the mismatch in the surface energy of the CuPc film with PTS- and OTS-modified dielectrics. Our study highlights that the positron annihilation technique, complemented by XRR, can be employed well for understanding buried interfaces required for organic electronic device applications.

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Notes

The authors declare no competing financial interest.

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